REMARKS

The application has been amended to place the application in condition for allowance at the time of the next Official Action.

A substitute Abstract of the Disclosure is provided to address the abstract objection noted in the Official Action.

Claims 90-109 were previously pending in the application. Claims 91-95, 97, 99-103, 105 and 107-109 were withdrawn from consideration as being directed to a non-elected species. Claims 91-95, 97, 99-103, 105 and 107-109 are canceled, leaving claims 90, 96, 98, 104 and 106 for consideration.

Claims 96 and 104 are amended to address the claim objection noted in the Official Action.

Claims 90, 96 and 106 are rejected as anticipated by SHIRAKI et al. 5,844,538. This rejection is respectfully traversed.

Claim 90 provides that a power supply electrode (of an analog amplifier) is connected to a scanning line. Accordingly, the power supply of the analog amplifier and the scanning line is shared. With such a structure, it is possible to attain high aperture efficiency.

In contrast, Figure 29 of SHIRAKI et al. shows that a separate power supply terminal is provided in buffer amplifying circuit 109.

As the reference does not disclose that which is recited, the anticipation rejection is not viable.

Claim 96 is a method claim that includes the same limitations of claim 90 and is also believed patentable over SHIRAKI et al.

Claim 106 depends from claim 90 and further defines the invention and is also believed patentable over SHIRAKI et al.

Claims 98 and 104 are rejected as unpatentable over SHIRAKI et al. This rejection is respectfully traversed.

Claim 98 is amended and includes similar recitations to claim 90 except the recitation of "scanning line" in claim 90 is "Nth scanning line" in claim 98. Claim 98 specifically provides that a power supply electrode is connected to an (N-1)th scanning line.

As set forth above, SHIRAKI et al. teach a separate power supply terminal provided in a buffer amplifying circuit. Accordingly, the advantages obtained by having this configuration are not taught by SHIRAKI et al. and thus claim 98 is not obvious in view of SHIRAKI et al. and is believed patentable over SHIRAKI et al.

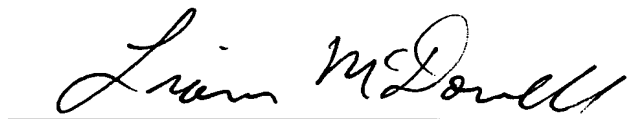
Claim 104 is a method claim that includes the limitations of claim 98. Therefore, for at least the reasons set forth above with respect to claim 98, claim 104 is also believed patentable over SHIRAKI et al.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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APPENDIX:

The Appendix includes the following item:

- amended Abstract of the Disclosure

ABSTRACT OF THE DISCLOSURE

~~The invention provides a~~ A high speed active matrix-type liquid crystal display device which can perform accurate gradation display for each one field (frame), by eliminating fluctuations in pixel voltage which accompany changes in capacitance of a liquid crystal. ~~The construction involves an active matrix type liquid crystal display device, wherein pixel electrodes are driven by MOS type transistor circuits respectively disposed in the vicinity of crossover points of a plurality of scanning lines 101 and a plurality of signal lines 102. Each of the MOS type transistor circuits comprises: an n-type MOS transistor 301 with a gate electrode connected to a scanning line 101, and one of a source electrode and a drain electrode connected to a signal line 102, a p-type MOS transistor 302 with a gate electrode connected to the source electrode or the drain electrode of the n-type MOS transistor 301 which is not connected to the signal line 102, and one of a source electrode and a drain electrode connected to the scanning line 101, and the other of the source electrode and the drain electrode connected to a pixel electrode 107, a voltage holding capacitor 106 formed between the gate electrode of the p-type MOS transistor 302 and a voltage holding capacitor electrode 105, and a~~

~~resistor connected between the pixel electrode 107 and the voltage holding capacitor electrode 105.~~ The device includes a pixel electrode and a MOS transistor circuit which drives the pixel electrode. The MOS transistor circuit is disposed in the vicinity of a cross-over point of a scanning line and a signal line, and includes a first MOS transistor in which a gate electrode is connected to the scanning line, and one of a source electrode and a drain electrode is connected to the signal line. The MOS transistor circuit also includes an analog amplifier in which an input electrode is connected to the other one of the source electrode and the drain electrode of the first MOS transistor, a power supply electrode is connected to the scanning line, and an output electrode is connected to the pixel electrode.